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Semiconductor Device Encapsulators, Methods of Encapsulating Semiconductor Devices and Methods of Forming Electronic Packages

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TECHNICAL FIELD

The invention pertains to methods of encapsulating semiconductor devices, such as, for example, methods of forming electronic packages, as well as to encapsulator devices.

BACKGROUND OF THE INVENTION

Semiconductor chips are frequently connected to a circuit board and subsequently encapsulated within a sealant compound to form a sealed package during semiconductor device manufacture. Among the methods that can be utilized for connecting chips to circuit boards are, for example, wire bonding, flip chip, chip on board, and tape automated bonding. All four methods can be followed by the application and curing of one or more liquid encapsulants over the chips and nearby circuitry. The cured encapsulants can protect the chips and their associated electronic interconnections to the boards from physical damage and ionic contamination.

The liquid encapsulants are typically applied by dispensing the encapsulants to form a glob over one or more chips and their associated electrical interconnections. Hence, the technology of providing such encapsulants is frequently referred to by the term "glob-top"

encapsulation. The encapsulants can be provided as single globs over single chips (so-called "single chip modules"), or as single globs encompassing multi-chip units (so-called "multi-chip modules").

Glob-top encapsulation was originally introduced for consumer packages such as, for example, video games, but the demand for miniaturized circuitry led to the use of glob-top as a preferred assembly method for many types of products including, for example, smart credit cards, and microprocessor circuitry. Glob-top encapsulation technology can enable manufacturers to make relatively thin devices, and also enables many companies to produce packages with cost equal to or less than conventional plastic packages. Typical glob-top compositions include epoxy or silicone encapsulating resins which provide protection against corrosion, vibration and mechanical stresses.

An exemplary automated process for applying a glob-top encapsulant to a chip is as follows. First, an integrated circuit chip is provided on a circuit board. The chip has exposed electrical leads (or pads) provided in electrical contact with corresponding leads (or pads) on the circuit board. The electrical connection can comprise, for example, a wire bond comprising exposed gold wires connecting the leads of the chip with those of the circuit board. Next, encapsulant is pumped through a single syringe to form a glob over the chip and over the electrical connections of the chip to the circuit board. Typically, the single syringe is moved relative to the chip as the encapsulant is

provided. In one method, the syringe is first moved to dispense encapsulant around a periphery of the chip and form a dam of encapsulant material. The syringe is then moved over a center of the chip to provide encapsulant onto the chip. The encapsulant provided onto the chip is prevented from flowing beyond the periphery of the chip by the dam that was initially provided. The encapsulant utilized for the dam can be different than that provided over a center of the chip. Specifically, the encapsulant utilized for forming the dam can be a so-called "dam" encapsulant and that provided over the center of the chip can be a so-called "fill" encapsulant. Dam encapsulants are generally more viscous than fill encapsulants. After the encapsulant is provided, it is cured by, for example, thermal processing to solidify the encapsulant material.

A continuing goal in semiconductor processing is to increase speed of semiconductor device fabrication. Accordingly, it would be desirable to increase the speed with which chips are encapsulated.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of encapsulating a semiconductor device. A semiconductor device is provided. A dispensing apparatus is provided proximate the semiconductor device. The dispensing apparatus has a plurality of

orifices. A liquid encapsulating material is dispensed through the plurality of orifices and over the semiconductor device.

In another aspect, the invention encompasses a method of forming an electronic package. A circuit board comprising a circuit pattern is electrically connected with a semiconductor device. A dispensing apparatus is provided proximate the semiconductor device. The dispensing apparatus has a plurality of dispensing orifices. A liquid encapsulating material is dispensed through the plurality of orifices and onto the semiconductor device. The encapsulating material is then cured.

In yet another aspect, the invention encompasses a semiconductor device encapsulator comprising a vessel configured for containing liquid encapsulant material, and a liquid dispensing apparatus in fluid communication with the vessel. The apparatus has a plurality of dispensing orifices. At least one of the dispensing orifices is configured for receipt over and within lateral confines of a semiconductor device being encapsulated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, perspective view of a preliminary step of a method of encapsulating semiconductor chips in accordance with the present invention. Fig. 1 illustrates a circuit board and an encapsulating material dispensing device.

Fig. 2 is a view of the Fig 1 encapsulating material dispensing device shown along the line 2-2 of Fig. 1.

Fig. 3 is a fragmentary, exploded top view of a portion of the Fig. 1 circuit board shown at a processing step subsequent to that of Fig. 1.

Fig. 4 is a view of the Fig. 3 fragment shown at a processing step subsequent to that of Fig. 3.

Fig. 5 is an exploded, fragmentary, top view of a portion of the Fig. 1 circuit board processed according to an alternative method of the present invention.

Fig. 6 is a view of the Fig. 5 fragment shown at a processing step subsequent to that of Fig. 5.

Fig. 7 is a view of the Fig. 5 fragment shown at a processing step subsequent to that of Fig. 6.

Fig. 8 is a diagrammatic, perspective view of a preliminary step of a second embodiment method of encapsulating semiconductor chips

in accordance with the present invention. Fig. 8 illustrates a circuit board and a second embodiment encapsulating material dispensing device.

Fig. 9 is an exploded top view of a portion of the Fig. 8 circuit board shown at a processing step subsequent to that of Fig. 8.

Fig. 10 is a view of the Fig. 9 circuit board shown at a processing step subsequent to that of Fig. 9.

Fig. 11 is a view of the Fig. 9 circuit board shown at a processing step subsequent to that of Fig. 10.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

An encapsulant forming apparatus (encapsulator) 10 encompassed by the present invention is described with reference to Fig. 1. Fig. 1 illustrates apparatus 10 positioned relative to a circuit board 12 having semiconductor devices 14 positioned thereon. Semiconductor devices 14 can comprise, for example, integrated circuit chips. Semiconductor devices 14 are in electrical connection with a circuit (not shown) provided on or within circuit board 12. In the shown embodiment, the electrical interconnection comprises wire bonding. Specifically, the interconnection comprises wires 16 (only some of which are labeled)

which electrically connect nodes (not shown) provided on or within semiconductor devices 14 with nodes (not shown) provided on or within circuit board 12. Wires 16 can comprise, for example, thin gold wires.

Apparatus 10 comprises a plurality of orifices 20 connected to a orifice support 22. Orifices 20 can comprise, for example, nozzles. Orifices 20 are in fluid connection with an inlet 24, which in turn is in fluid connection with a liquid encapsulant source 26. Inlet 24 can comprise, for example, tubing that is chemically inert relative to the liquid encapsulant material flowed through inlet 24. Source 26 can comprise a vessel configured to contain a liquid encapsulant material. In operation, liquid encapsulant is flowed from source 26, through inlet 24, and out of orifices 20. The flow of liquid encapsulant material can be powered by conventional methods, such as, for example, a pump (not shown) provided between source 26 and inlet 24. Additionally, valves can be provided between orifices 20 and source 26 to control flow of material out of orifices 20. In the shown embodiment, all of orifices 20 are connected to a common source 26. It is to be understood, however, that the invention encompasses alternative embodiments wherein one or more of orifices 20 are connected to a different encapsulant source than are others of orifices 20. Utilization of different encapsulant sources can enable different encapsulants to be flowed through different orifices.

Apparatus 10 can further comprise a table (not shown) configured to retain circuit board 12 in precise alignment with orifices 20.

Fig. 2 is a view of apparatus 10 along the line 2-2 of Fig. 1. Fig. 2 illustrates a preferred embodiment of apparatus 10 comprising five outlet orifices 20. One of outlet orifices 20 is interiorly located relative to the remaining four outlet orifices 20. Such interiorly located outlet orifice 20 will provide encapsulant onto a semiconductor device 14, while the remaining outlet orifices 20 provide encapsulant around a periphery of semiconductor device 14. Such is illustrated in Fig. 3, wherein a fragment of circuit board 12 is illustrated after dispensing of an encapsulant material 30 through orifices 20 (Fig. 2).

The encapsulant material 30 in Fig. 3 is provided as a series of five drops in locations corresponding to the locations of outlet orifices 20 of Fig. 2. Such five drops comprise a single drop 31 interiorly located on semiconductor device 14, and four drops 33 around a periphery of device 14. Drop 31 is from the interiorly located dispensing orifice 20 received over and within lateral confines of the semiconductor device 14 being encapsulated. Drops 33 are from dispensing orifices 20 received outside of lateral confines of the semiconductor device 14 being encapsulated.

The five separate drops of encapsulant material 30 can be formed, for example, by simultaneously dispensing encapsulant material 30 through all five of orifices 20 (Fig. 2). Alternatively, the five drops can

be formed sequentially by dispensing encapsulant material non-simultaneously through orifices 20. For instance, drops 33 at the periphery of device 14 can be dispensed first to form a dam around device 14, and subsequently interiorly located drop 31 can be dispensed over device 14.

Referring to Fig. 4, the wafer fragment of Fig. 3 is illustrated after further dispensing of liquid encapsulant material 30 from orifices 20. Liquid encapsulant 30 now encapsulates an entirety of semiconductor device 14 (shown in phantom) and the wires 16 (shown in phantom). Encapsulant 30 thus forms a glob-top over semiconductor device 14. Encapsulant 30 can next be cured by, for example, thermal processing, to solidify encapsulant 30 into a protective coating adhered over semiconductor device 14 and wires 16.

Fig. 5 illustrates an alternative method of the present invention wherein encapsulant 30 is distributed about a periphery of semiconductor device 14 prior to dispensing encapsulant 30 onto a central region of semiconductor device 14. The dispense pattern of Fig. 5 can be formed by, for example, utilizing the orifice arrangement of Fig. 2 and rotating either support structure 22, circuit board 12, or both as encapsulant material is dispensed from the peripherally located orifices 20. Alternatively, the dispense pattern of Fig. 5 can be formed by utilizing an apparatus 10 having a different orifice arrangement than that illustrated in Fig. 2. Such different orifice arrangement could, for

example, correspond to a plurality of orifices arranged in a pattern corresponding to that of the dispensed encapsulant shown in Fig. 5.

Referring to Fig. 6, the wafer fragment of Fig. 5 is illustrated after provision of sufficient encapsulant to form a dam 32 around semiconductor device 14.

Referring to Fig. 7, the circuit board fragment of Fig. 6 is shown after provision of an encapsulant material within a center of dam 32 (Fig. 6) to overlay semiconductor device 14 (shown in phantom). The encapsulant provided to overlay device 14 can be dispensed from one or more interiorly located orifices of an encapsulant dispensing device analogous to the device 10 of Figs. 1 and 2. The encapsulant provided within the center of dam 32 can comprise the same encapsulant material as that utilized for forming dam 32, or a different material. Utilization of a different material can enable the material of dam 32 to have a different viscosity than that utilized to overlay semiconductor device 14. For instance, the material utilized for dam 32 can be a so-called "dam" encapsulant and that utilized over device 14 can be a so-called "fill" encapsulant.

After provision of encapsulant material over device 14, a glob 36 comprising the encapsulant material over device 14 and the material of dam 32 (Fig. 6) is formed to encapsulate device 14 and the wires 16 extending to device 14. The encapsulated semiconductor device 14 and circuit board 12 together comprise an electronic package.

A second embodiment encapsulant dispensing apparatus 50 is described with reference to Fig. 8. Apparatus 50 comprises four spaced sets (52, 54, 56 and 58) of dispensing orifices (52a, 54a, 56a and 58a) configured as a linear array. Each of the orifice sets is in fluid communication with a liquid encapsulant source 60. Orifice sets 52, 54, 56 and 58 can comprise, for example, the orifice configuration described above with reference to the apparatus 10 of Figs. 1 and 2. It is noted that the invention encompasses other embodiments (not shown) wherein the spaced orifice sets are replaced with spaced single orifices. Also, although each of the shown orifice sets comprises the same number and arrangements of orifices, the invention encompasses other embodiments (not shown) wherein some of the orifice sets comprise a different number and/or arrangement of orifices than other orifice sets.

A circuit board 70 is shown in Fig. 8. Circuit board 70 comprises semiconductor devices 72, 74, 76, 78, 82, 84, 86 and 88. Semiconductor devices 72, 74, 76, and 78 form a first array of four devices, and semiconductor devices 82, 84, 86 and 88 form a second array of four devices. The array of dispensing orifice sets 52, 54, 56 and 58 is provided such that each of the individual orifice sets 52, 54, 56 and 58 is in correspondence with individual semiconductor devices of the first array of semiconductor devices. Specifically, orifice set 52 is in correspondence with semiconductor device 72, orifice set 54 is in correspondence with semiconductor device 74, orifice set 56 is in

correspondence with semiconductor device 76, and orifice set 58 is in correspondence with semiconductor device 78.

Fig. 9 shows circuit board 70 after a liquid encapsulating material 90 is dispensed through the orifices of sets 52, 54, 56 and 58. Liquid encapsulant material 90 can be dispensed simultaneously through all of orifice sets 52, 54, 56 and 58, or sequentially through one or more of the sets. In the embodiment of Fig. 9, the encapsulant material is provided around a periphery of each of semiconductor devices 72, 74, 76 and 78, as well as over each of semiconductor devices 72, 74, 76 and 78. Such pattern is identical to that described above with reference to Fig. 3. Variations of the encapsulant dispensing can be conducted in accordance with variations discussed above with reference to Figs. 3 and 5. Specifically, the encapsulant provided around the peripheries of one or more devices 72, 74, 76 and 78 can be provided prior to encapsulant being provided over one or more of devices 72, 74, 76 and 78, or after such provision. Also, one or more of orifices 52a, 54a, 56a and 58a can be moved relative to semiconductor devices 72, 74, 76 and 78 during dispensing of encapsulant material 90. Such moving can comprise either moving circuit board 70 during the dispensing, moving one or more of orifice sets 52, 54, 56 and 58 during the dispensing, or moving both circuit board 70 and one or more of orifice sets 52, 54, 56 and 58 during the dispensing.

Referring to Fig. 10, additional encapsulant 90 is provided relative to semiconductor wafer 72, 74, 76 and 78 (shown in phantom) to form globs of encapsulant which entirely encapsulate semiconductor devices 72, 74, 76 and 78.

Referring to Fig. 11, the array of orifice sets 52, 54, 56 and 58 (Fig. 8) is moved relative to circuit board 70 to align the array with semiconductor devices 82, 84, 86 and 88. Subsequently, encapsulant 90 is flowed over semiconductor devices 82, 84, 86 and 88 to form encapsulating globs over such devices. The movement of the array of orifice sets, 52, 54, 56 and 58 relative to circuit board 70 can comprise, for example, either moving orifice sets 52, 54, 56 and 58, moving circuit board 70, or moving both orifice sets 52, 54, 56 and 58 and circuit board 70.

In the shown embodiment of Figs. 8-11, all of orifices 52a, 54a, 56a and 58a dispense a common encapsulant material. However, it is to be understood that the invention encompasses other embodiments (not shown) wherein one or more of orifices 52a, 54a, 56a and 58a dispense a different encapsulant from remaining orifices 52a, 54a, 56a and 58a. Such alternative embodiments can comprise, for example, utilizing a different encapsulant to form dams analogous to the dam 32 of Fig. 6 around one or more of semiconductive devices 72, 74, 76, 78, 82, 84, 86 and 88 prior to providing encapsulant on or over a center of such devices.

In the above-discussed embodiments, the semiconductor devices comprise rectangular shapes, and more specifically comprise square shapes. However, it is to be understood that the invention encompasses other embodiments wherein the semiconductor devices comprise other shapes. The configuration of orifices utilized to provide encapsulant relative to such other shaped semiconductor devices can be adapted to provide encapsulant both around a periphery of the devices and over the devices. Also, it is noted that although the above-described drawings illustrate dispensing of encapsulant at peripheries of semiconductor devices as well as over the devices, the invention encompasses other embodiments (not shown) where an encapsulant is dispensed only over a device, or only at a periphery of a device. In such other embodiments the encapsulant can be dispensed and then subsequently flowed from over the device to the periphery, or from the periphery to over the device, so that both the device and the interconnects at the device periphery are encapsulated.

In the embodiment shown in Figs. 8-11, the array of orifice sets 52, 54, 56 and 58 is a linear array. However, the invention encompasses other embodiments (not shown) wherein the array is non-linear. For instance, the array could be a matrix. An exemplary matrix comprises eight orifice sets configured in four columns having two rows each.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.